

What is claimed is:

1. A Semiconductor integrated circuit comprising:

a nonvolatile memory to store address information
indicating a relationship between an address of a first

5 memory space and an address of a second memory space;

a plurality of functional modules each to has an
address in the second memory space; and

a bus control circuit,

wherein the bus control circuit receives a first
10 address in the first memory space and translates the first
address into a second address in the second memory space
using the address information and access is made to a
functional module having the second address among the
plurality of functional modules.

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2. The semiconductor integrated circuit according to claim
1, further comprising:

a bus; and

a switching circuit to control a connection between
20 the plurality of functional modules and the bus,

wherein:

the nonvolatile memory stores connect/disconnect
information for the plurality of functional modules; and

the switching circuit selects a functional module to be connected with the bus according to the connect/disconnect information.

- 5 3. The semiconductor integrated circuit according to claim 1, wherein the address information is stored in the nonvolatile memory when a probing test is conducted on the semiconductor integrated circuit.
- 10 4. The semiconductor integrated circuit according to claim 2, wherein the connect/disconnect information is stored in the nonvolatile memory when a probing test is conducted on the semiconductor integrated circuit.